IDEC Chip Design Contest

A RISC-V Based Ibex Core Implementation in 28nm Process

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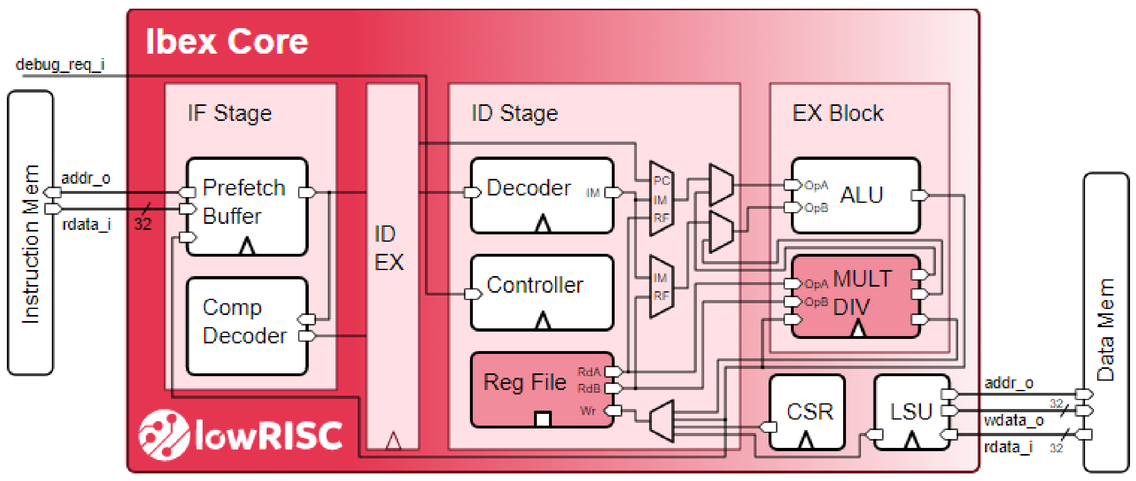
1. Introduction

In today's self-powered IoT area, circuits consuming ultra-low current are attracting the biggest attention. Especially in AIoT area, the devices contain the microcontroller process sensed data without communication of data. Therefore, recent IoT devices require a low-power processor. A presented processor based on an open-source Ibex core consumes low power and small area, enough to be applied to self-power AIoT devices.

2. A design of Ibex RISC-V core

2.1 Architecture of ibex RISC-V core

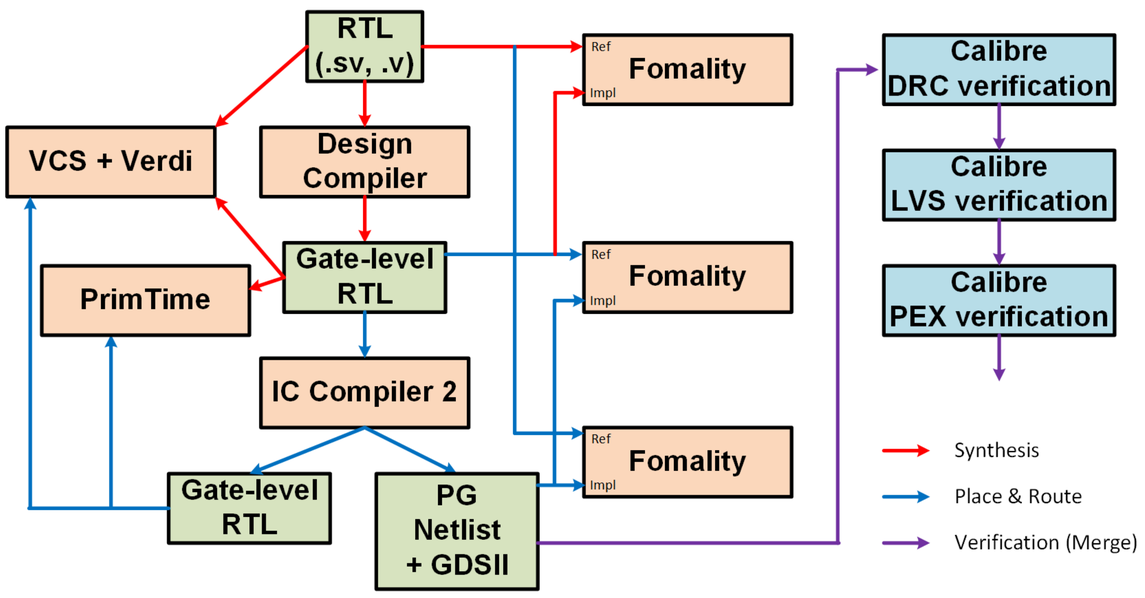


The ibex RISC-V core consists of instruction memory, data memory, and a four-stage pipeline arithmetic core. All of the memories and interfaces are implemented in FPGA, only the core is implemented in the chip. And the core supports 5 kinds of extensions below.

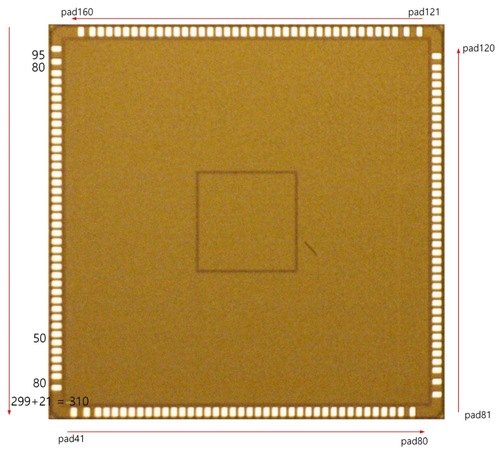
Extension	Version	Configurability
C: Standard Extension for Compressed Instructions	2.0	always enabled
M: Standard Extension for Integer Multiplication and Division	2.0	optional
B: Standard Extension for Bit-Manipulation Instructions	1.0.0	optional
Zicsr: Control and Status Register Instructions	2.0	aways enabled
Zifencei: Instruction-Fetch Fence	2.0	always enabled

3. Chip implementation and Test

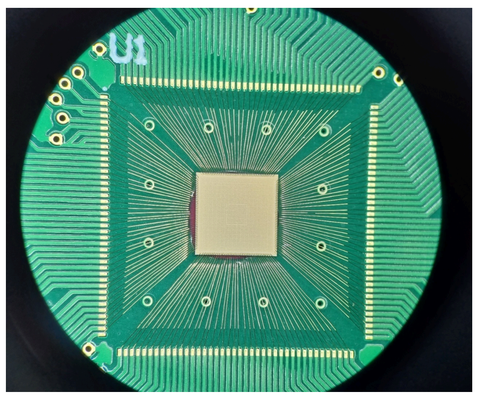
3.1 How to implement ibex RISC-V core



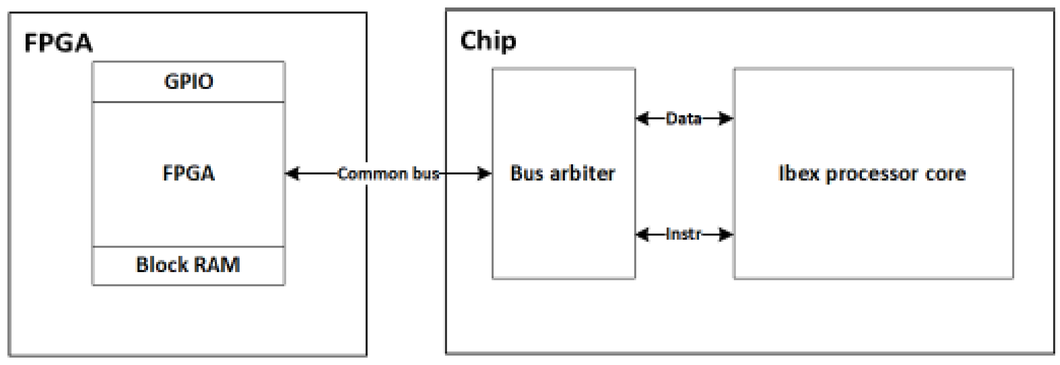
3.2 Die photography

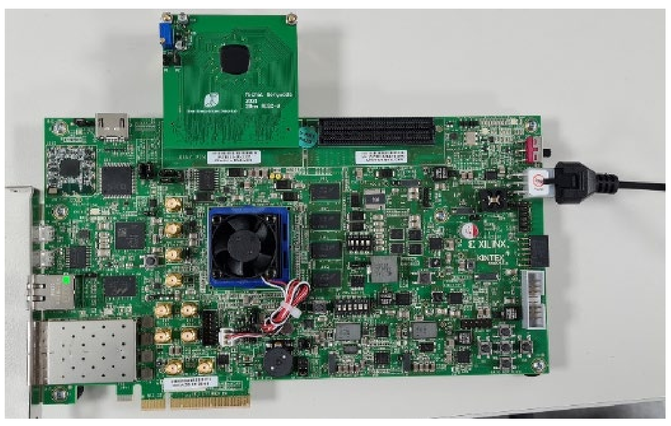


3.3 PCB photography



3.4 Test setup





3.5 Test result of Ibex RISC-V core

The Ibex RISC-V core is verified in RTL-level simulation. However, in a real chip test condition, the core cannot be verified. This is why there are so many pins to be connected. Some of the signals could not be connected to FPGA board successfully due to FPGA board using multiple devices on the same line. In future work, we will try to test chip with FPGA having more pins.

4. Conclusion

In future works, it is crucial to reduce the number of IO pads by integrating the memory and peripherals into the chip. In addition, the memory should have external programming interface such ad JTAG.

5. Acknowledgement

The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.

6. Reference

[1] lowRISC, "Ibex Documentation" [Online] Available: http://ibex_core.readthedocs.io/en/latest/01_overveiw/index.html